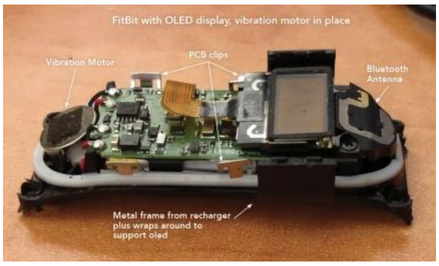
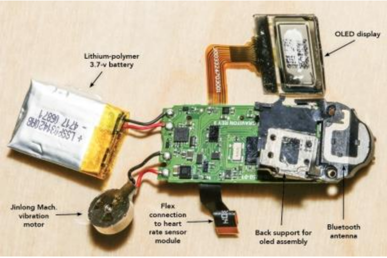
PACKAGING OF INTELLIGENT SYSTEMS

Prof. Vivek Subramanian

Modern Integrated Systems

- **Silicon is king for integrating intelligence**
- **Lots of sensors and physical world interfaces**
- **Energy needs strongly impact form factor**





Discussion Topic 1

What are the constraints impacting packaging of systems containing the following:

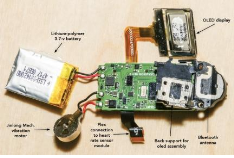
- Display / Touch Screen
- Battery
- Microprocessors
- Memory

INTEGRATION OF INTELLIGENCE

Hierarchical Assembly – what and why?

- **Building systems by combining components with varying complexity to produce a highly integrated system**
- **Why?**

It is expensive to build a robot that can move large distances at high-precision. Therefore, it is better to do things in a hierarchy of assembly



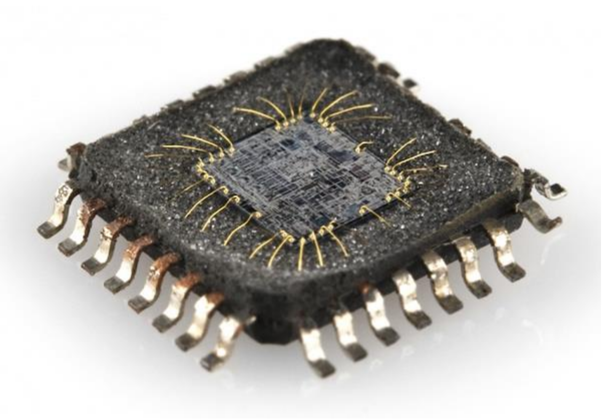
Silicon wafer cost: ~\$10,000 for a 300mm diameter wafer
Area: ~70,000 mm^2
Cost: ~\$150,000 per m^2

Precision hierarchy:
On-wafer (transistors): 2nm
On-wafer (wiring): 100nm
Wafer-to-package: 1μm
Package: 10μm
Board: 100μm

The hierarchy in microelectronics

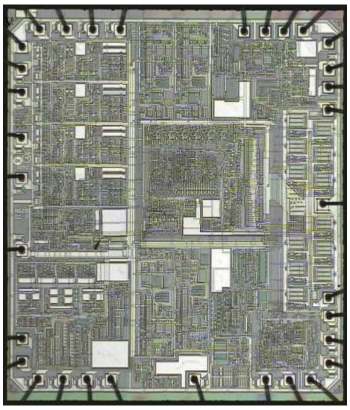
The Board Level

The hierarchy in microelectronics



Inside the chip package

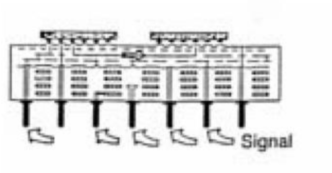
The hierarchy in microelectronics



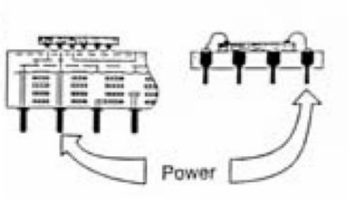
The semiconductor Die

Packaging of silicon integrated circuits – why?

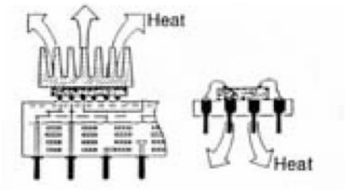
Signal distribution



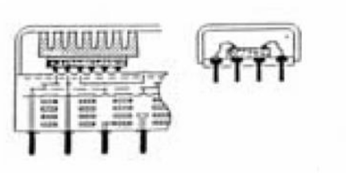
Power distribution



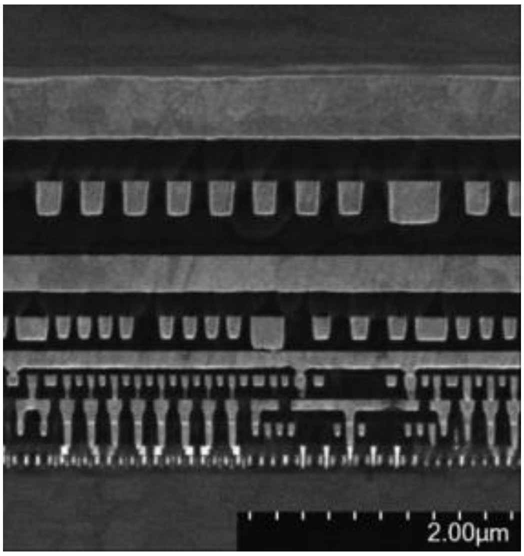
Heat dissipation (cooling)

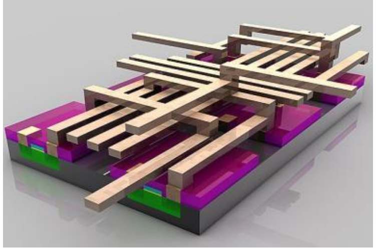


Protection (mechanical, chemical, electromagnetic)



Cross-section of a microprocessor

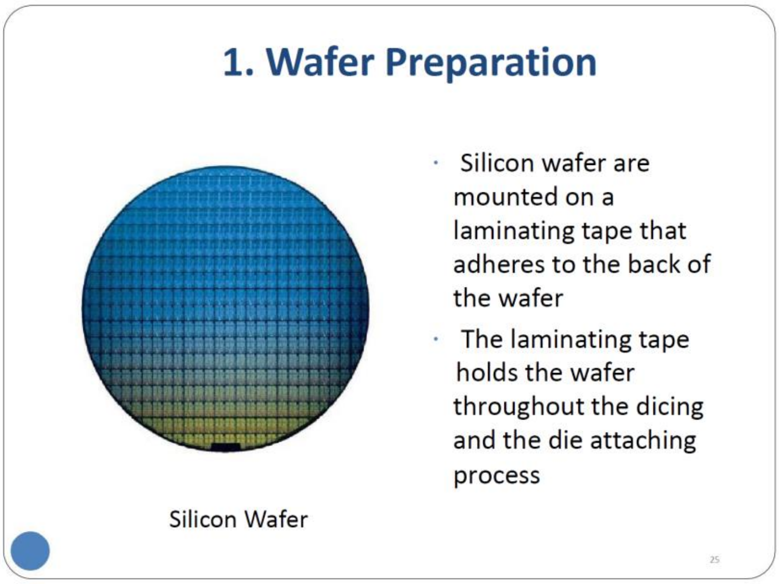




Questions to consider

- **What is the peak process temperature that such a wafer can be subjected to? Why?**
  - **HINT: Consider the materials inside the fully fabricated chip**

Chip Packaging Process Flow Major Steps

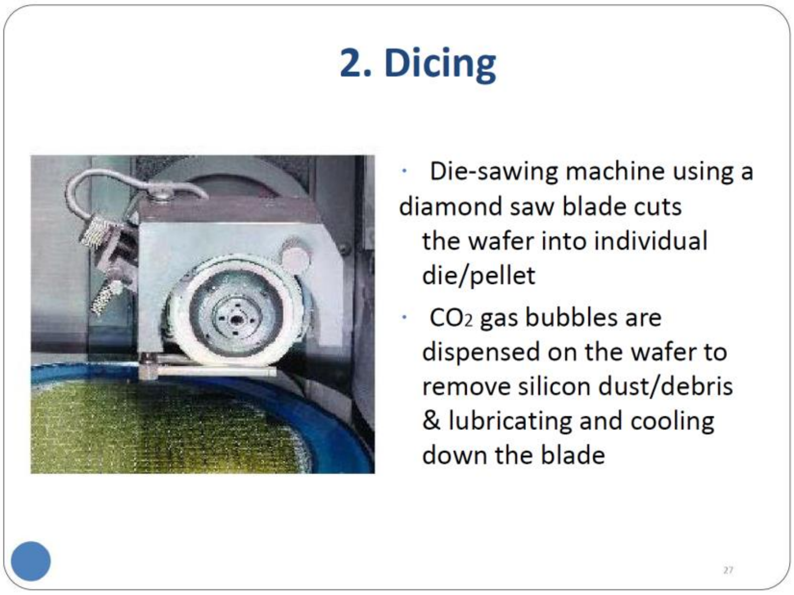


1. Wafer Preparation

- Silicon wafer are mounted on a laminating tape that adheres to the back of the wafer
- The laminating tape holds the wafer throughout the dicing and the die attaching process

Silicon Wafer

Chip Packaging Process Flow Major Steps

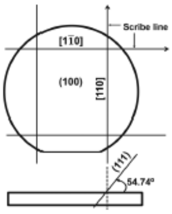


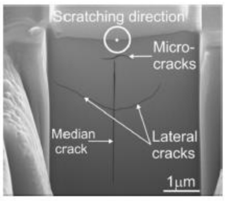
2. Dicing

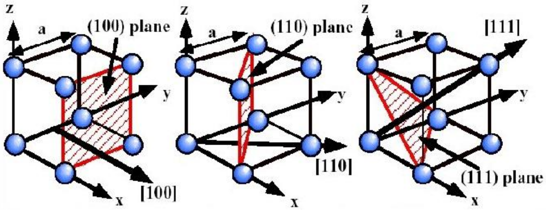
- Die-sawing machine using a diamond saw blade cuts the wafer into individual die/pellet
- CO_2 gas bubbles are dispensed on the wafer to remove silicon dust/debris & lubricating and cooling down the blade

Die singulation Technologies – Scribing / Cleaving

- **A "scratch" is made along a crystal plan, and upon application of mechanical pressure, the wafer cleaves along the plane**







Discussion: Advantages and disadvantages of cleaving

Singulation Technology: Sawing

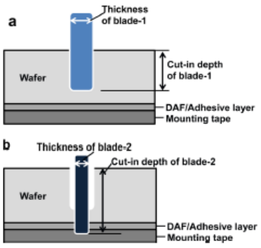
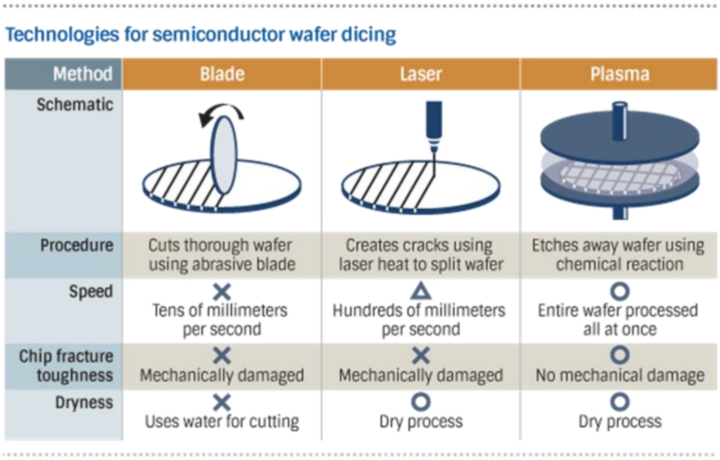


FIG. 6. (Color online) Schematic two-step blade dicing process. (a) Step 1: dicing partially into wafer substrate; (b) step 2: dicing into mounting tape.

Singulation Technology: Laser and Plasma cutting



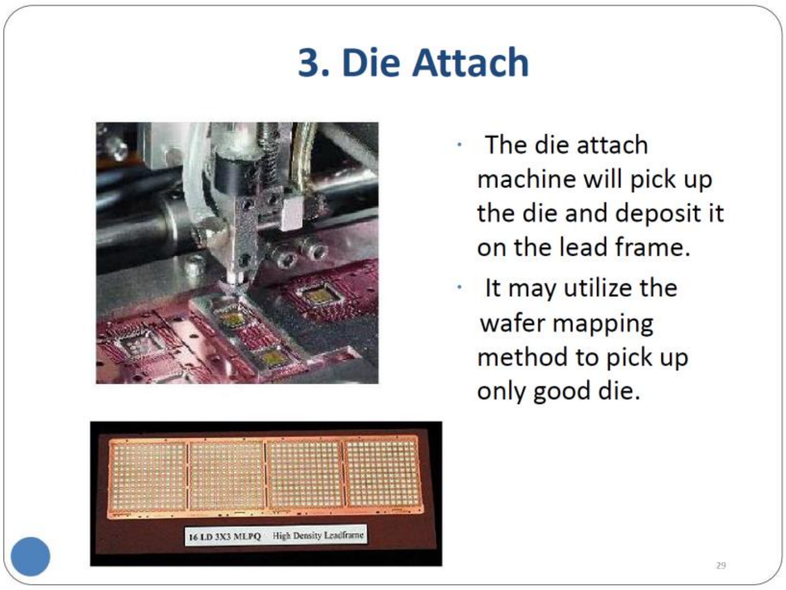
Technologies for semiconductor wafer dicing

Method	Blade	Laser	Plasma
Schematic			
Procedure	Cuts thorough wafer using abrasive blade	Creates cracks using laser heat to split wafer	Etches away wafer using chemical reaction
Speed	✕ Tens of millimeters per second	△ Hundreds of millimeters per second	○ Entire wafer processed all at once
Chip fracture toughness	✕ Mechanically damaged	✕ Mechanically damaged	○ No mechanical damage
Dryness	✕ Uses water for cutting	○ Dry process	○ Dry process

General Considerations during singulation

- Size of kerf
- Chipping
- Die sidewall damage
- Surface contamination
- ESD
- Delamination
- Intra-die defects

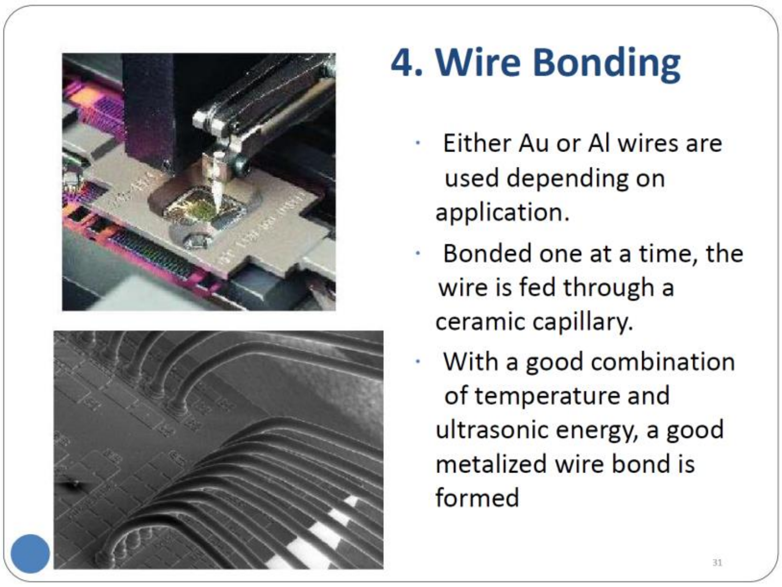
Chip Packaging Process Flow Major Steps



3. Die Attach

- The die attach machine will pick up the die and deposit it on the lead frame.
- It may utilize the wafer mapping method to pick up only good die.

Chip Packaging Process Flow Major Steps

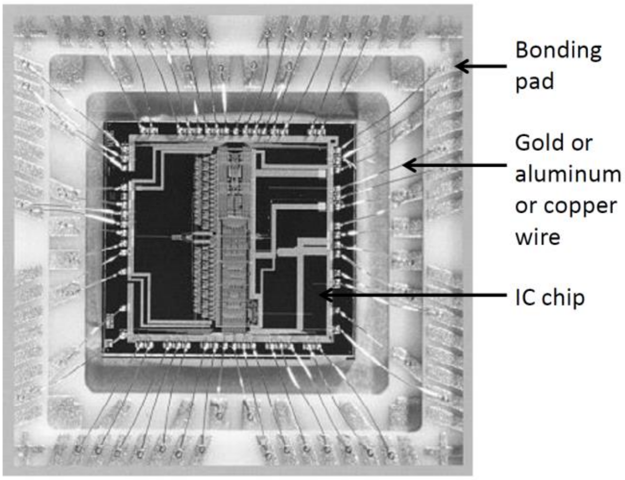


4. Wire Bonding

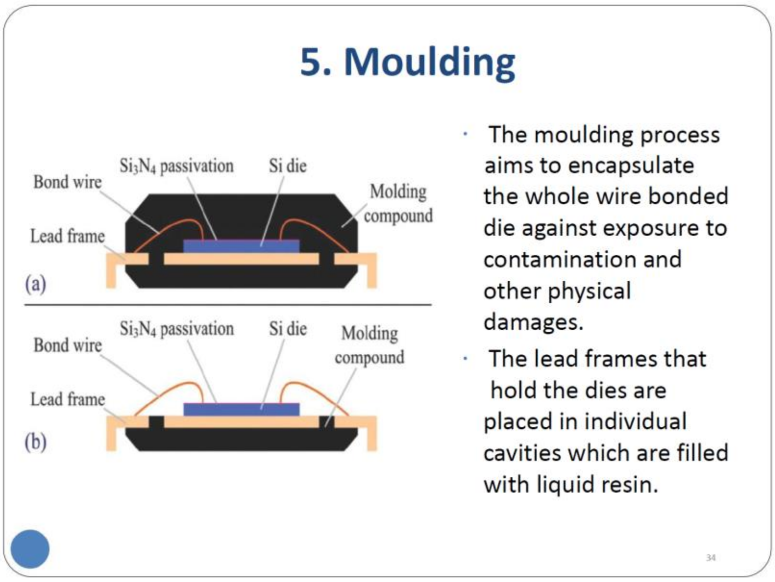
- Either Au or Al wires are used depending on application.
- Bonded one at a time, the wire is fed through a ceramic capillary.
- With a good combination of temperature and ultrasonic energy, a good metalized wire bond is formed

Chip Packaging Process Flow Major Steps

Wire-bonding



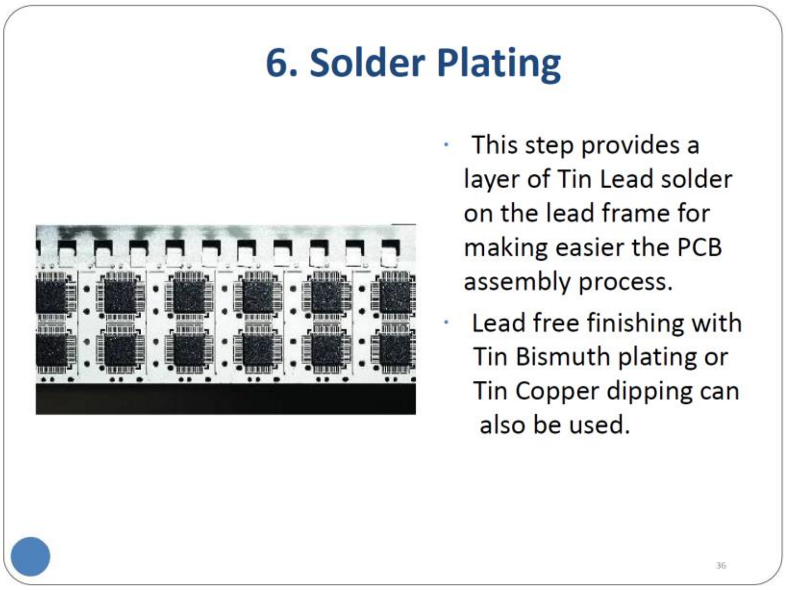
Chip Packaging Process Flow Major Steps



5. Moulding

- The moulding process aims to encapsulate the whole wire bonded die against exposure to contamination and other physical damages.
- The lead frames that hold the dies are placed in individual cavities which are filled with liquid resin.

Chip Packaging Process Flow Major Steps



6. Solder Plating

- This step provides a layer of Tin Lead solder on the lead frame for making easier the PCB assembly process.
- Lead free finishing with Tin Bismuth plating or Tin Copper dipping can also be used.

Solder Choices

Leaded VS Lead-Free Solder

63/37 Solder in air

SAC Solder in air

Leaded Solder:
-Tin-lead ($Sn_{63}Pb_{37}$)
-melting point ~183 °C
-shiny & smooth surface

Lead-Free Solder:
-Tin-Silver-Copper ($SnAgCu$)
-melting range of 217–220˚C
-slightly grainy surface
Others: $SnCu$

What is a solder

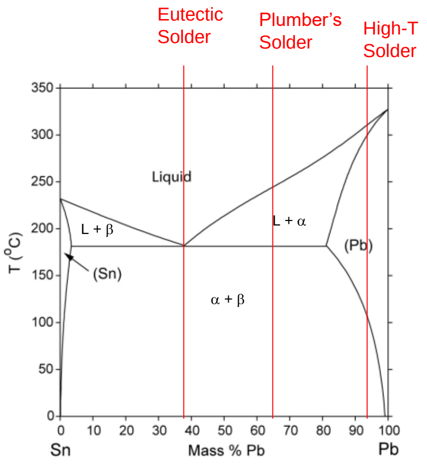
- **Fundamentally, a solder is a low-melting-temperature conductive material (typically a metal alloy)**
  - **Low temperature to ensure package and PCB compatibility**
  - **Conductive to deliver low interconnection resistance**
  - **Wettability to ensure good contact to pads on both sides**
  - **Chemical and thermal stability (including dissolution of pads) for reliability**
- **Most important solders are based on tin alloys**

Selected solder prices in 2015 [72].

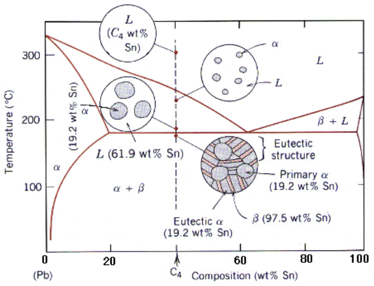
Alloy	$US/kg (approx.)
Sn37Pb	14
Sn9Zn	21
Sn5Sb	21
Sn56Bi	17
Sn0.7Cu	21
SAC305	41
Sn2Ag0.5Cu7.5Bi	34
Sn2.5Ag0.8Cu0.5Sb	37
Sn3.5Ag3Bi	44
Sn3.4Ag4.8Bi	43
Sn3.5Ag	44
Sn4Ag0.5Cu	47
Sn3.5Ag1.5In	50
Sn2.8Ag20In	118

The classic solder: Pb-Sn

- **How do we choose the alloy ratio?**



How to consider solidification of solder



Consider a 40 wt% Sn-60 wt% Pb alloy on the phase diagram.

Part 1:

- At 183.1 degrees C, just above the eutectic line, what phase(s) is (are) present?

Find the point corresponding to 40 wt% Sn and 183.1 degrees C on the diagram. It lies in an alpha + liquid region. Therefore both the alpha phase and the liquid phase are present.

- what is (are) the compositions of the phase(s)?

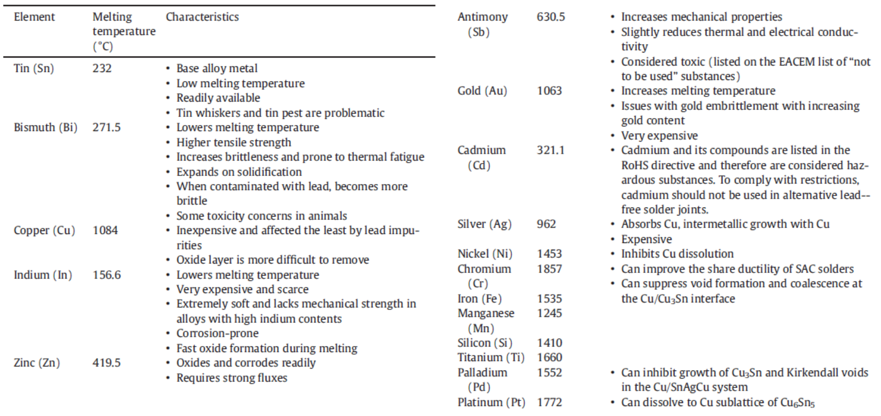
Extend a horizontal line from this point to the closest phase boundaries. The composition of the liquid phase is 61.9 wt% Sn and the composition of the alpha phase is 19.2 wt% Sn.

Part 2:

- Now, the temperature is lowered slightly to right below the eutectic line at 182.9%. What is the composition of each phase?

Drop the lines from the intersections as before to discover that the composition of the alpha phase is 19.2 wt% Sn and the composition of the beta phase is 97.5% wt% Sn.

General choices for adding to Tin



Element	Melting temperature (°C)	Characteristics
Tin (Sn)	232	• Base alloy metal • Low melting temperature • Readily available • Tin whiskers and tin pest are problematic
Bismuth (Bi)	271.5	• Lowers melting temperature • Higher tensile strength • Increases brittleness and prone to thermal fatigue • Expands on solidification • When contaminated with lead, becomes more brittle • Some toxicity concerns in animals
Copper (Cu)	1084	• Inexpensive and affected the least by lead impurities • Oxide layer is more difficult to remove
Indium (In)	156.6	• Lowers melting temperature • Very expensive and scarce • Extremely soft and lacks mechanical strength in alloys with high indium contents • Corrosion-prone • Fast oxide formation during melting
Zinc (Zn)	419.5	• Oxides and corrodes readily • Requires strong fluxes
Antimony (Sb)	630.5	• Increases mechanical properties • Slightly reduces thermal and electrical conductivity • Considered toxic (listed on the EACEM list of "not to be used" substances)
Gold (Au)	1063	• Increases melting temperature • Issues with gold embrittlement with increasing gold content • Very expensive
Cadmium (Cd)	321.1	• Cadmium and its compounds are listed in the RoHS directive and therefore are considered hazardous substances. To comply with restrictions, cadmium should not be used in alternative lead--free solder joints.
Silver (Ag)	962	• Absorbs Cu, intermetallic growth with Cu • Expensive
Nickel (Ni)	1453	• Inhibits Cu dissolution
Chromium (Cr)	1857	• Can improve the share ductility of SAC solders • Can suppress void formation and coalescence at the Cu/Cu_3Sn interface
Iron (Fe)	1535	
Manganese (Mn)	1245	
Silicon (Si)	1410	
Titanium (Ti)	1660	
Palladium (Pd)	1552	• Can inhibit growth of Cu_3Sn and Kirkendall voids in the Cu/SnAgCu system
Platinum (Pt)	1772	• Can dissolve to Cu sublattice of Cu_6Sn_5

Pb-Free Solders

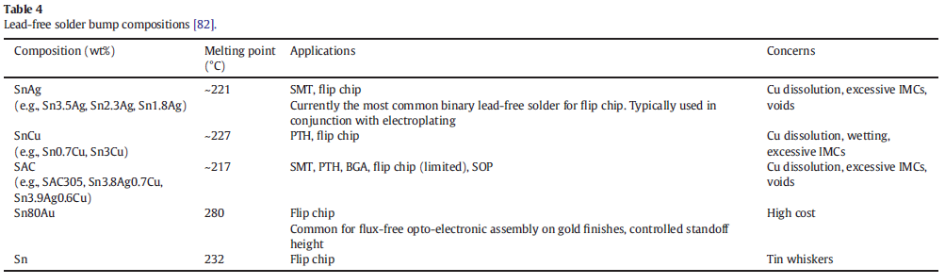
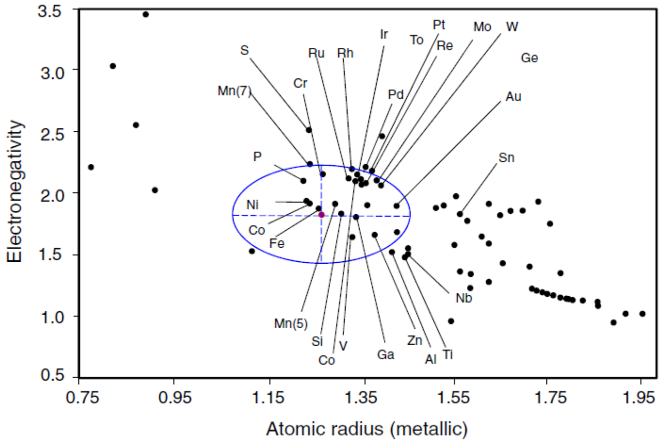


Table 4
Lead-free solder bump compositions [82].

Composition (wt%)	Melting point (°C)	Applications	Concerns
SnAg (e.g., Sn3.5Ag, Sn2.3Ag, Sn1.8Ag)	~221	SMT, flip chip Currently the most common binary lead-free solder for flip chip. Typically used in conjunction with electroplating	Cu dissolution, excessive IMCs, voids
SnCu (e.g., Sn0.7Cu, Sn3Cu)	~227	PTH, flip chip	Cu dissolution, wetting, excessive IMCs
SAC (e.g., SAC305, Sn3.8Ag0.7Cu, Sn3.9Ag0.6Cu)	~217	SMT, PTH, BGA, flip chip (limited), SOP	Cu dissolution, excessive IMCs, voids
Sn80Au	280	Flip chip Common for flux-free opto-electronic assembly on gold finishes, controlled standoff height	High cost
Sn	232	Flip chip	Tin whiskers

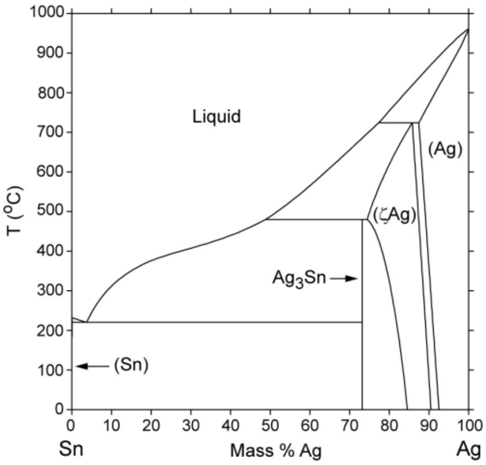
Cu solubility



Darken-Gerry plot… atoms with similar electonegativity and radius will typically show higher solid solubility

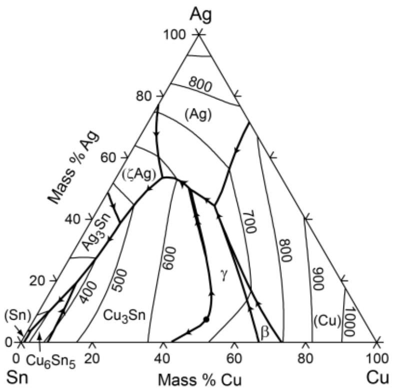
Sn-Ag

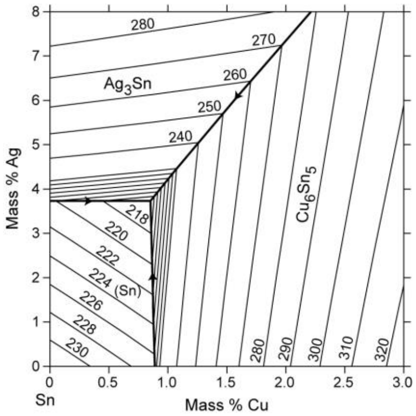
- **What are the key advantages / disadvantages?**



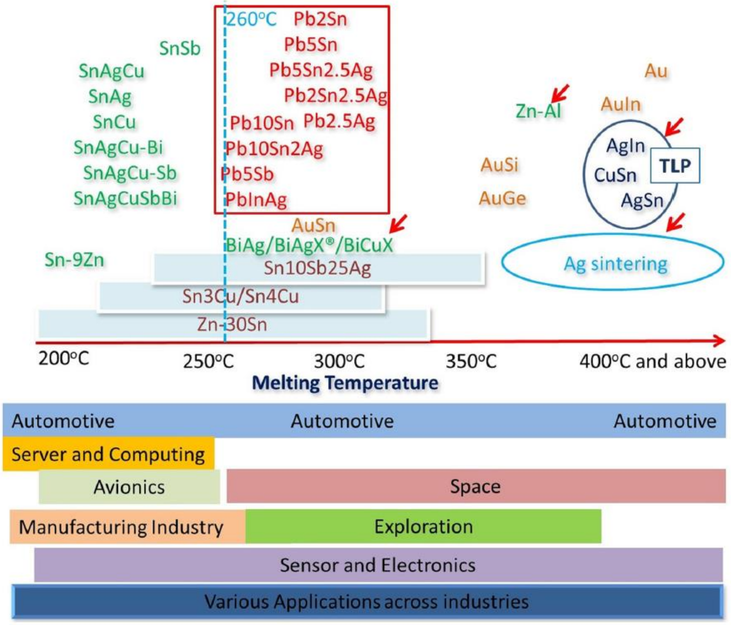
The Sn-Ag-Cu system

- **Why?**

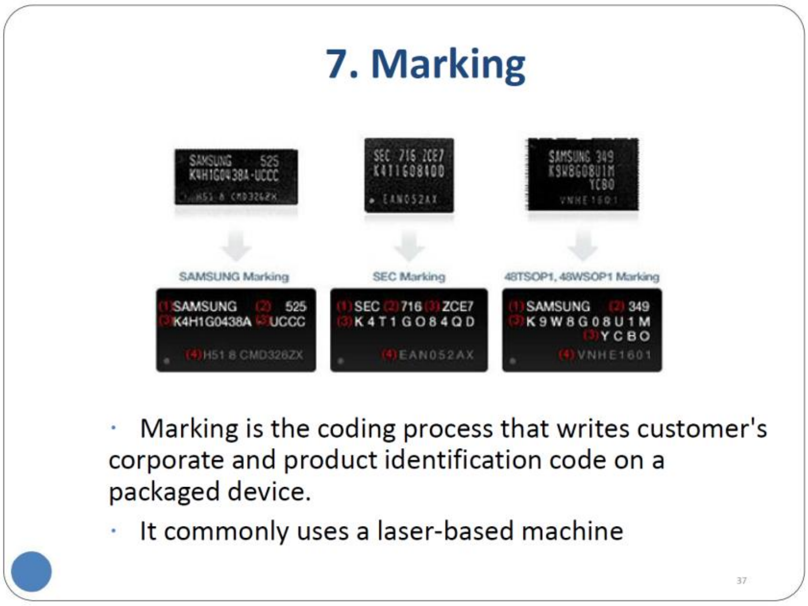




Summary of Solder Choices



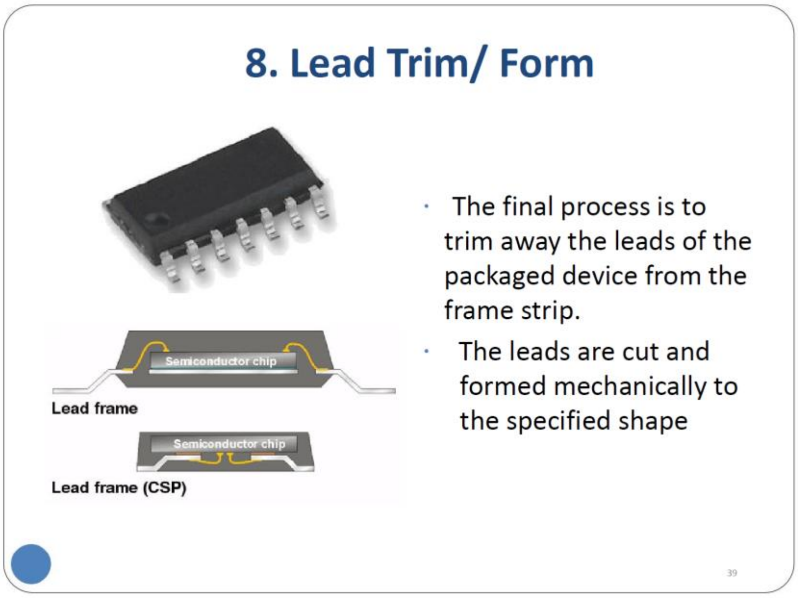
Chip Packaging Process Flow Major Steps



7. Marking

- Marking is the coding process that writes customer's corporate and product identification code on a packaged device.
- It commonly uses a laser-based machine

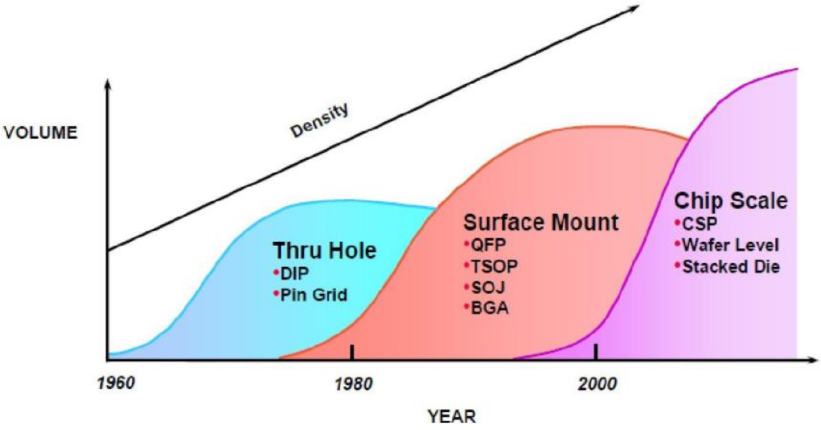
Chip Packaging Process Flow Major Steps



8. Lead Trim/ Form

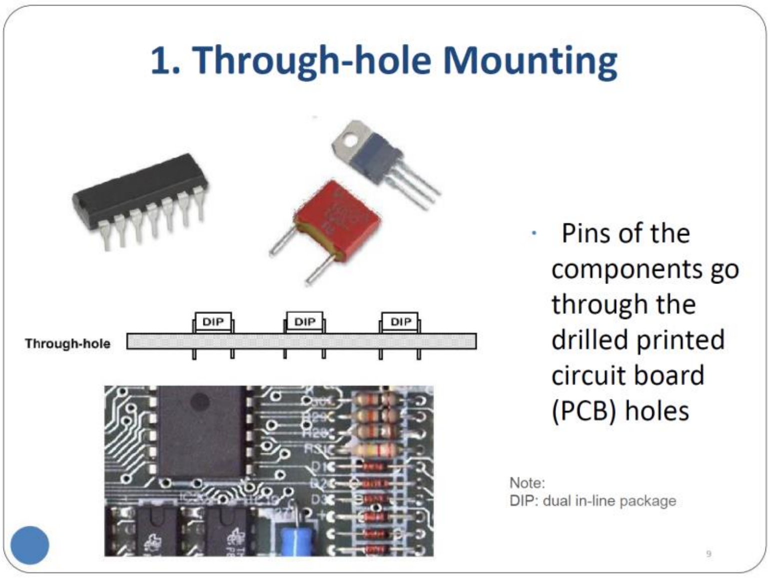
- The final process is to trim away the leads of the packaged device from the frame strip.
- The leads are cut and formed mechanically to the specified shape

Packaging Trends over time?



Question: What was the major technology platform during each transition?

Packaging Wave 1: 1960s to today

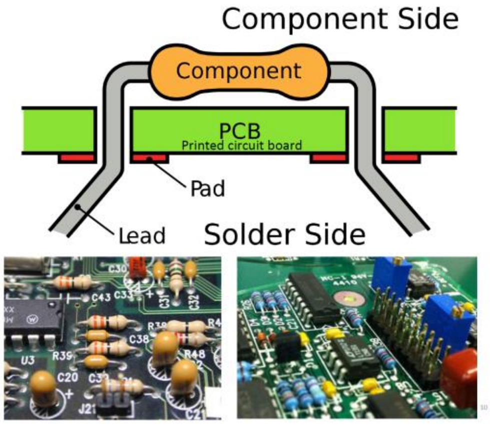


1. Through-hole Mounting

- Pins of the components go through the drilled printed circuit board (PCB) holes

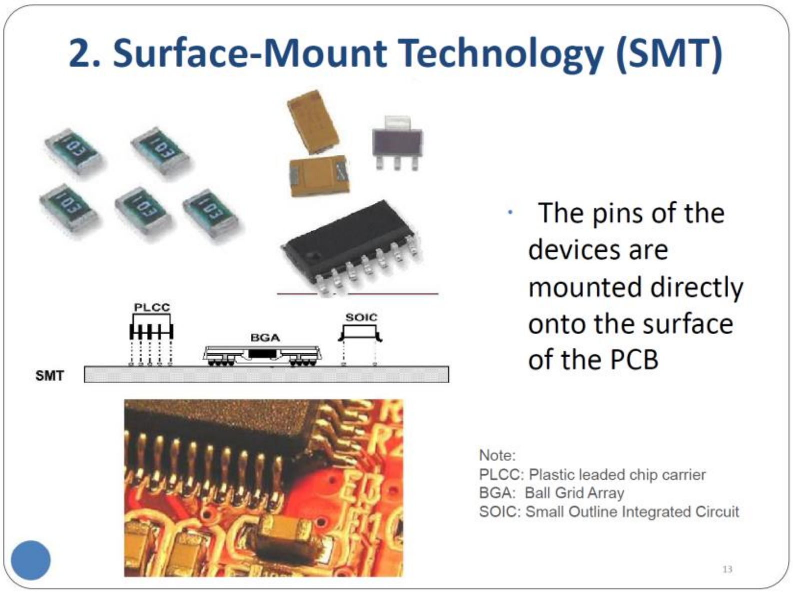
Note:
DIP: dual in-line package

Packaging Wave 1: 1960s to today



What are the advantages / disadvantages of through-hole packaging?

Packaging Wave 2: 1980s to today

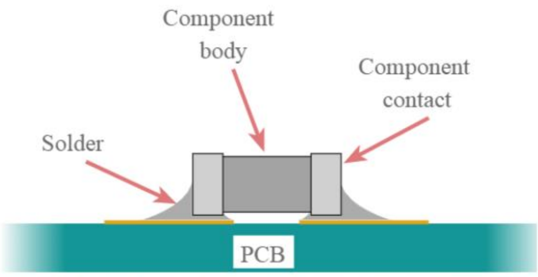


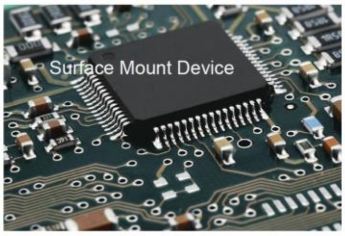
2. Surface-Mount Technology (SMT)

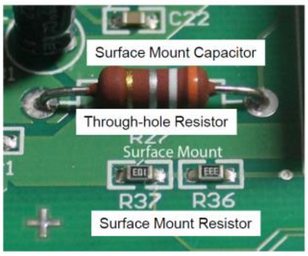
- The pins of the devices are mounted directly onto the surface of the PCB

Note:
PLCC: Plastic leaded chip carrier
BGA: Ball Grid Array
SOIC: Small Outline Integrated Circuit

Packaging Wave 2: 1980s to today



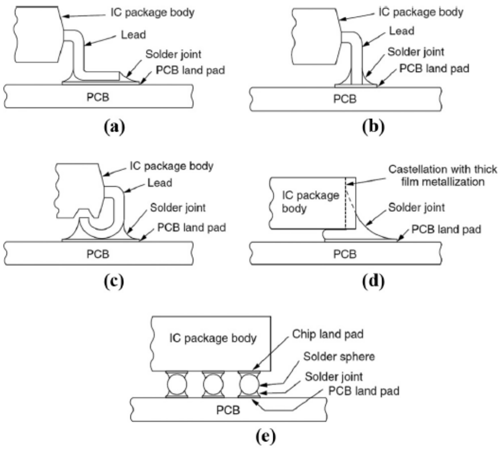




What are the advantages / disadvantages of surface mounting?

Solder deposition processes for surface mount components

- **General configurations**



Notes: (a) gullwing; (b) butt-lead; (c) J-lead; (d) leadless metallization; (e) ball-lead

Solder deposition processes for surface mount components

Figure 3 Reflow soldering process

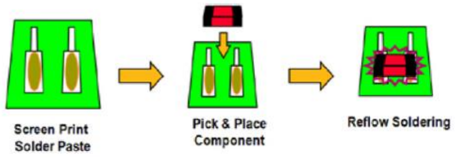
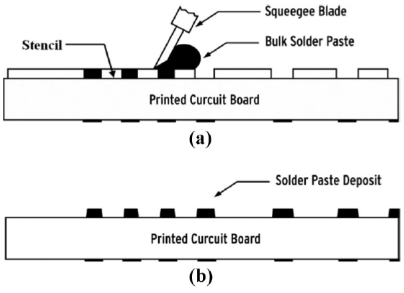
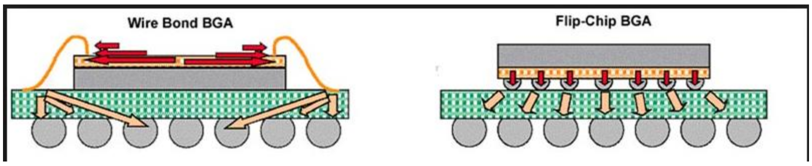


Figure 4 Stencil printing process



Major Chip Interconnection Types



Comparison Flip-chip vs wirebond

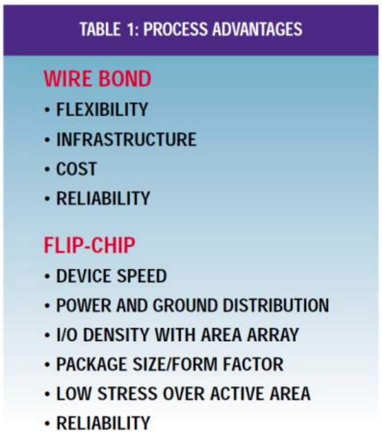


TABLE 1: PROCESS ADVANTAGES

WIRE BOND
- FLEXIBILITY
- INFRASTRUCTURE
- COST
- RELIABILITY

FLIP-CHIP
- DEVICE SPEED
- POWER AND GROUND DISTRIBUTION
- I/O DENSITY WITH AREA ARRAY
- PACKAGE SIZE/FORM FACTOR
- LOW STRESS OVER ACTIVE AREA
- RELIABILITY

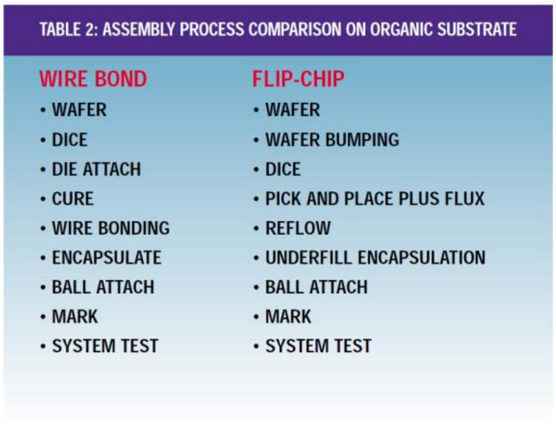
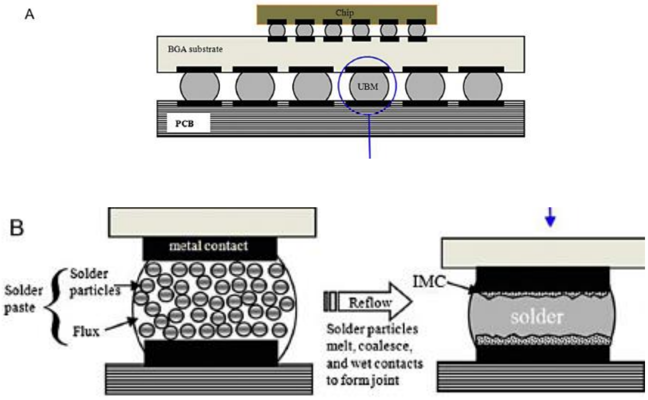


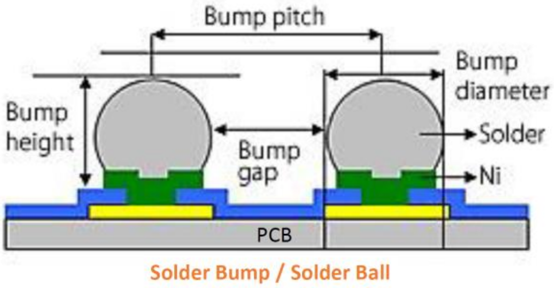
TABLE 2: ASSEMBLY PROCESS COMPARISON ON ORGANIC SUBSTRATE

WIRE BOND	FLIP-CHIP
• WAFER	• WAFER
• DICE	• WAFER BUMPING
• DIE ATTACH	• DICE
• CURE	• PICK AND PLACE PLUS FLUX
• WIRE BONDING	• REFLOW
• ENCAPSULATE	• UNDERFILL ENCAPSULATION
• BALL ATTACH	• BALL ATTACH
• MARK	• MARK
• SYSTEM TEST	• SYSTEM TEST

Solder Pastes



Dimensions in packaging



Solder Bump / Solder Ball

Question: Why do we need solder bumps?

Non-planarity and solders

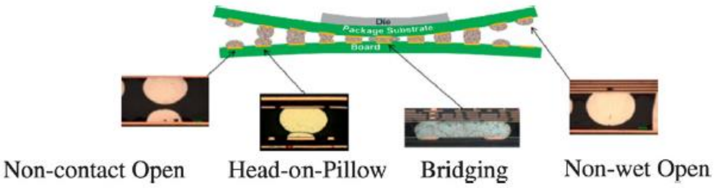
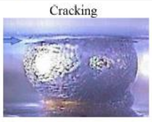
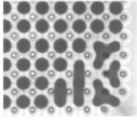


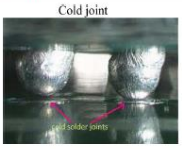
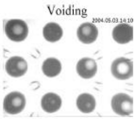
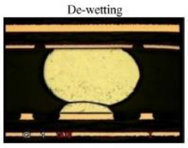
Fig. 5. Typical surface mount technology defects.

Preview: Exercise

- **Develop a framework to estimate the amount of nonplanarity allowed as a function of pad density**

Some defect types in solder ball packaging

Defect type	Mechanism (s)
Cracking 	Too high an internal stress due to fast temperature change rate
Tombstoning & Skewing 	Uneven wetting at both ends of chip
Bridging & Hot Slump 	Viscosity drops with temperature
Opens 	Non-wetting due to oxidation

Defect type	Mechanism (s)
Cold joint 	Insufficient coalescence
Voiding 	Excessive oxidation
De-wetting 	Overheat at temperature above solder melting point

Bump vs. Pillar

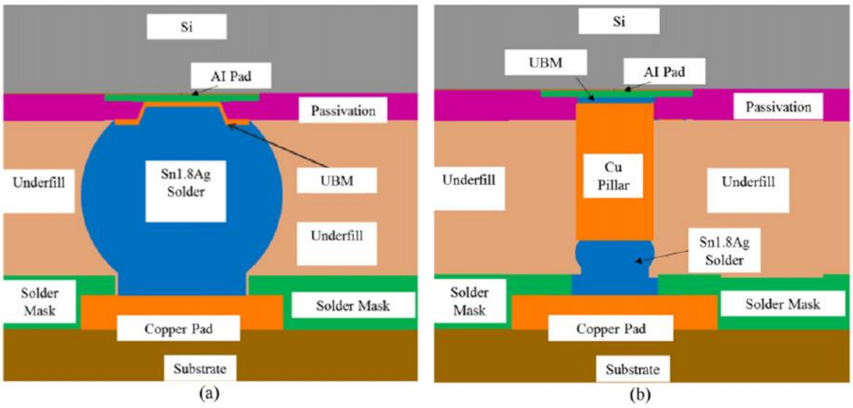
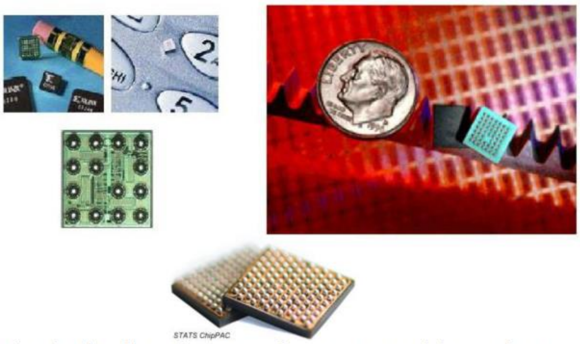


Fig. 7. Schematic of conventional (a) and Cu pillar (b) SnAg solder bumps [148].

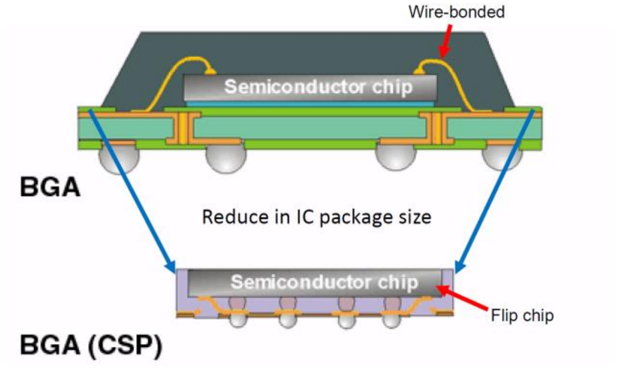
Packaging Wave 3: 2000s to today

3. Chip Scale Packages (CSP)

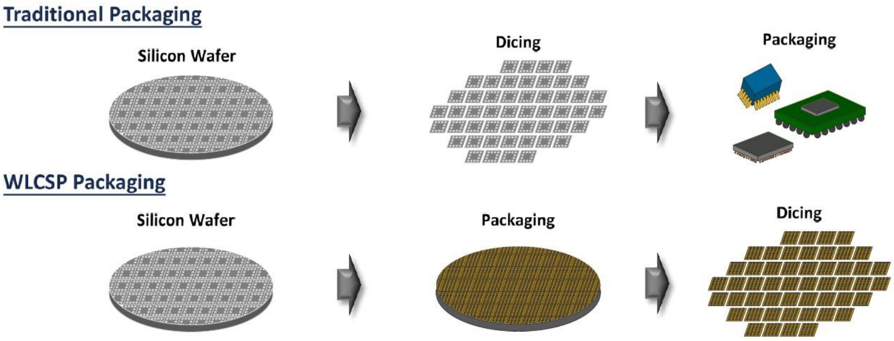


- CSP is single-die, direct surface mountable package
- Is an evolution of surface mount device (SMD)
- CSP come in many forms –flip chip, wire-bonded, ball grid array, leaded, etc.

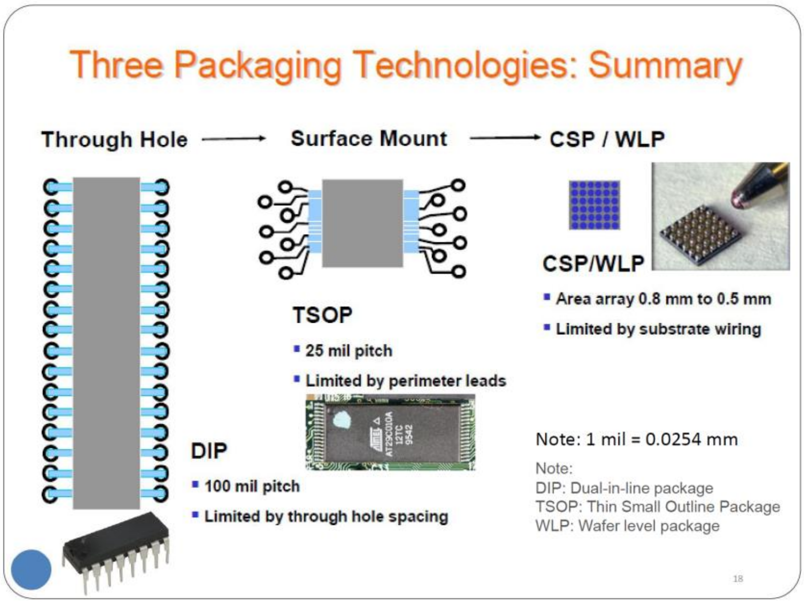
Packaging Wave 3: 2000s to today



Packaging of Silicon Wafers



Density trends in packaging



Three Packaging Technologies: Summary

Through Hole ⟶ Surface Mount ⟶ CSP / WLP

TSOP
- 25 mil pitch
- Limited by perimeter leads

CSP/WLP
- Area array 0.8 mm to 0.5 mm
- Limited by substrate wiring

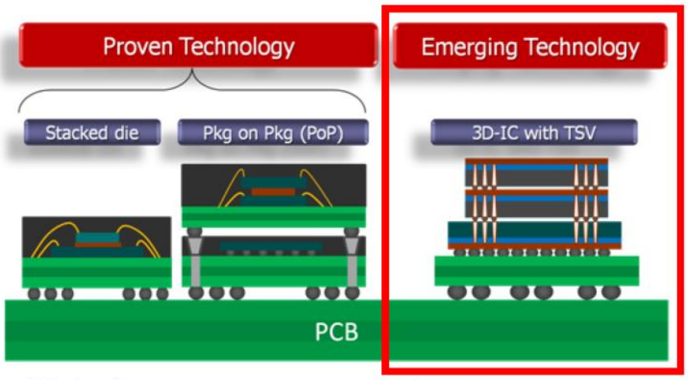
DIP
- 100 mil pitch
- Limited by through hole spacing

Note: 1 mil = 0.0254 mm

Note:
DIP: Dual-in-line package
TSOP: Thin Small Outline Package
WLP: Wafer level package

Chip Stacking: Enabling Wearables and Mobile

Recent IC Packaging Technology – 3D IC with TSV

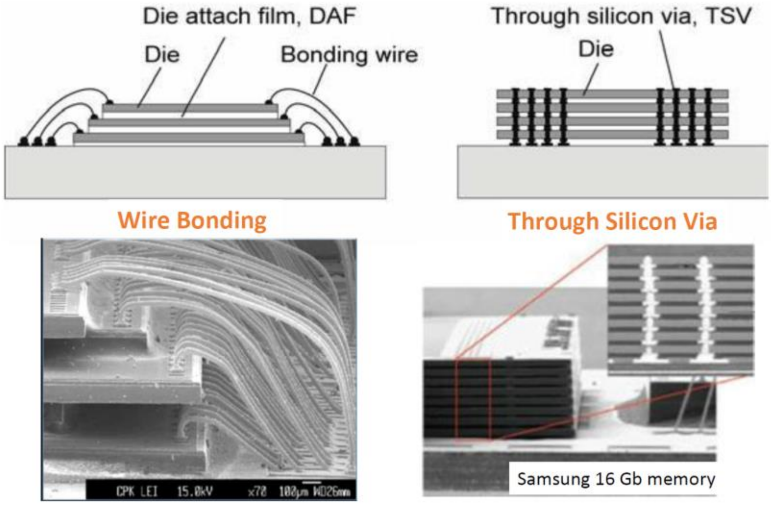


*Wire bonding
*Flip chip bump:
Diameter: ~100 µ meter
Pitch: ~100 µ meter

*Through Silicon Via
*Micro bump:
Diameter: ~10 µ meter
Pitch: ~10 µ meter

Chip Stacking

Wire Bonding VS Through Silicon Via



Samsung 16 Gb memory

Review Thought Exercise

- **Design a wearable device for monitoring your sweat, focusing on component choices and impact on packaging**